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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/820,484
Filing Date: April 08, 2004
Appellant(s): KELLY, MICHAEL G.

Lawrence D Maxwell
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 3/12/2008 appealing from the Office action mailed 5/07/2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,143,865	HIDESHIMA	09-1992
5,665,655	WHITE	09-1997

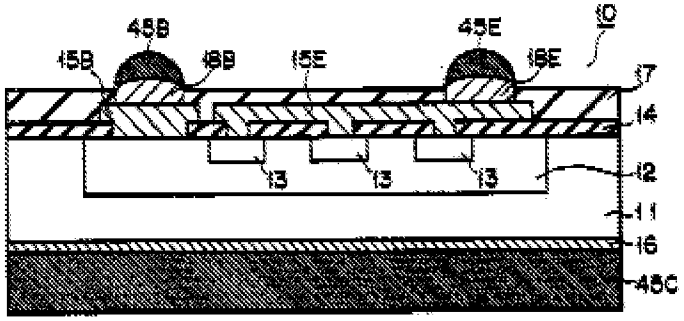
5,977,626	WANG	11-1999
2003/0067057	WU	04-2003
6,717,267	KUNIKIYO	04-2004
6,853,070	KHAN	02-2005

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-9 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over anticipated by Hideshima et al. (US 5,143,865) in view of Wu (2003/0067057).

Regarding claim 1, Hideshima (e.g. fig. 8) shows an integrated circuit system, comprising: a die 11 incorporating an integrated circuit and having a top side and a bottom side, the top side supporting an electrical signal communication metallization 15 b/e wherein the bottom side supporting a bottom side thermal dissipation metallization 16/43C but does not disclose a top side thermal dissipation metallization.



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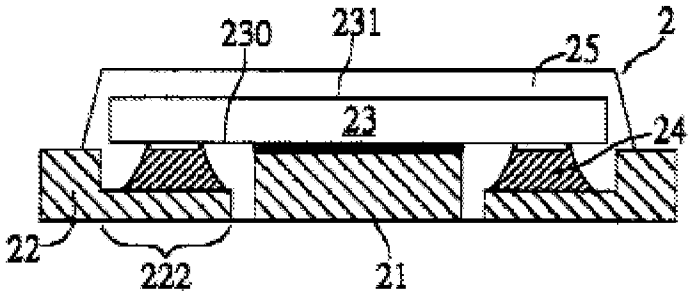
Nevertheless, Wu (e.g. fig. 3A) shows a die a topside thermal dissipation metallization 21. This type of embodiment allows the heat generated from a semiconductor chip to be quickly dissipated through a die pad of the lead frame after the

semiconductor chip is attached to the die pad, so as to improve overall heat dissipating efficiency of the semiconductor package (pp 0009).

FIG. 3A



It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a top side thermal dissipation metallization layer as disclosed by Wu to allow the heat generated from a semiconductor chip to be quickly dissipated through a die pad of the lead frame after the semiconductor chip is attached to the die pad, so as to improve overall heat dissipating efficiency of the semiconductor package as suggested by Wu.

Regarding claim 2, Hideshima shows that the electrical signal communication metallization comprises a plurality of exposed bonding elements on the top side of the die.

Regarding claim 3, Hideshima shows that the bonding elements are contained in a peripheral region of the topside of the die.

Regarding claim 4, Wu shows that the topside thermal dissipation metallization is disposed in a central region of the topside of the die.

Regarding claim 5, Wu shows that the topside thermal dissipation metallization is surrounded by the plurality of boning elements.

Regarding claim 6, White shows that the electrical signal communication metallization surrounds the top side thermal dissipation metallization.

Regarding claim 7, Hideshima shows that the topside thermal dissipation metallization comprises a patterned metal layer.

Regarding claim 8, Hideshima shows that the patterned metal layer comprises at least one through-hole.

Regarding claim 9, Hideshima shows that the patterned metal layer comprises an array of through-holes.

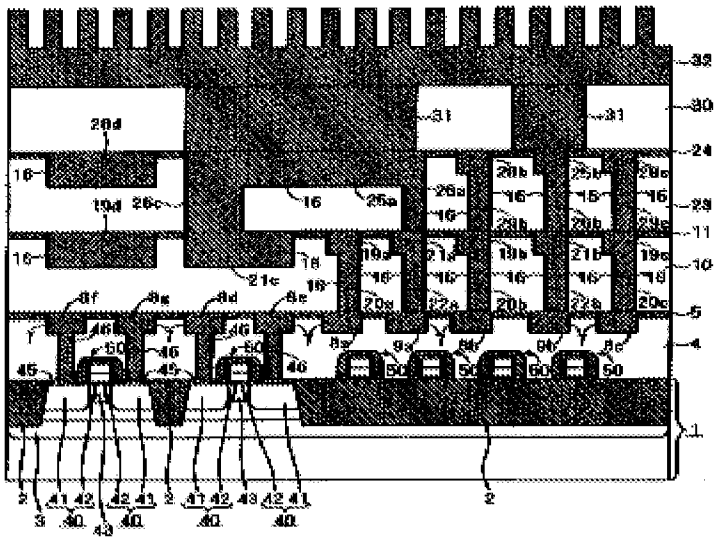
Regarding claim 21, Wu shows that the electrical signal communication metallization is free of any direct electrical connection to the top side thermal dissipation metallization on the top side of the die.

Claims 1-4 and 6-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over anticipated by Hideshima et al. (US 5,143,865) in view of Kunikiyo (US 6,717,267).

Regarding claim 1, Hideshima shows an integrated circuit system, comprising: a die 11 incorporating an integrated circuit and having a top side and a bottom side, the top side supporting an electrical signal communication metallization 15 b/e wherein the bottom side supporting a bottom side thermal dissipation metallization 16/43C but does not disclose a top side thermal dissipation metallization. Nevertheless, Kunikiyo (e.g. fig. 19) shows a top side thermal dissipation metallization 31. According to Kunikiyo, this type of mounting structure provides more satisfactory effect of cooling away the heat in the interlayer insulating films than conventional semiconductor devices having no dummy interconnections or dummy plugs, since metal has higher thermal conducting rate than the

interlayer insulating films. This improves the circuit operation of the semiconductor device (col. 23/lls. 1-18).

FIG. 19



It would have been obvious to one of ordinary skill in the art at the time the invention was made to include in Hideshima's invention a topside thermal dissipation metallization such as dummy patterns in accordance to Kunikiyo's invention to improve the circuit operation since the heat can be satisfactorily removed form the interlayer insulating films.

Regarding claim 2, Hideshima shows that the electrical signal communication metallization comprises a plurality of exposed bonding elements on the top side of the die.

Regarding claim 3, Hideshima shows that the bonding elements are contained in a peripheral region of the topside of the die.

Regarding claim 4, Kunikiyo shows that the topside thermal dissipation metallization is disposed in a central region of the topside of the die.

Regarding claim 6, Kunikiyo shows that the electrical signal communication metallization surrounds the topside thermal dissipation metallization (e.g. plugs).

Regarding claim 7, Kunikiyo shows that the topside thermal dissipation metallization comprises a patterned metal layer.

Regarding claim 8, Hideshima shows that the patterned metal layer comprises at least one through-hole.

Regarding claim 9, Hideshima shows that the patterned metal layer comprises an array of through-holes.

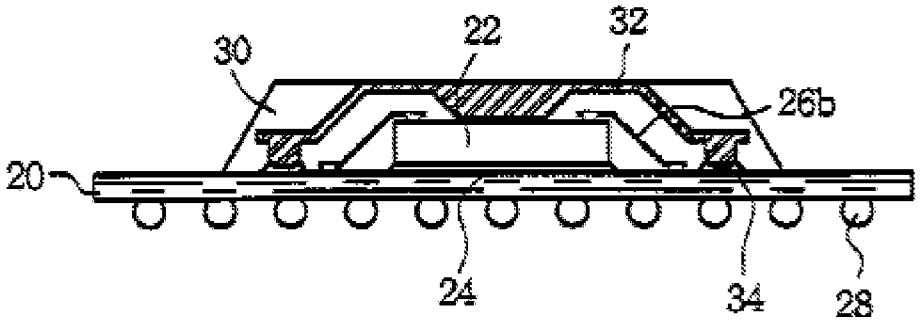
Regarding claim 10, Kunikiyo shows a top heat spreader 32 metallurgically bonded to the op side thermal dissipation metallization of the die.

Regarding claim 11, Kunikiyo shows that the integrated circuit is connected electrically to the op side heat spreader by an electrical path extending through the top side thermal dissipation metallization.

Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over anticipated by Hideshima et al. (US 5,143,865) in view of Kunikiyo (US 6,717,267) further in view of Wang (US 5,977,626).

Regarding claim 12, Hideshima in view of Kunikiyo shows most aspects of the instant invention except for an electrical interface and a substrate containing a wiring interconnection between the electrical signal communication metallization and the electrical interface. Nevertheless, Wang (e.g. fig. 4) shows a package having a good efficiency of spreading heat and enhanced EM shielding that includes an electrical interface 28 and a substrate 20 containing a wiring interconnection between the electrical

signal communication metallization and the electrical interface (col. 1/lls. 11-33; col. 2/lls. 10-14 & col. 3/lls. 10-12).



It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the package disclosed by Wang to package the device disclosed by Hideshima in view Kunikiyo, which includes an electrical interface and a substrate containing a wiring interconnection between the electrical signal communication metallization and the electrical interface, because this package structure has a good efficiency of spreading heat and enhanced EM shielding as taught by Wang.

Regarding claim 13, Wang shows a top heat spreader 32 mounted on the substrate and forms a lid of the package covering the topside of the die.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over anticipated by Hideshima et al. (US 5,143,865) in view of Kunikiyo (US 6,717,267) further in view of Khan et al. (US 6,853,070).

Regarding claim 14, Hideshima in view of Kunikiyo shows most aspects of the instant invention including a package including a bottom layer 45C metallurgically bonded (i.e. metal to metal bond) to the bottom side thermal dissipation metallization 16 of the die but does not explicitly disclose that the second layer 45C is a heat spreader.

Nevertheless, Khan (e.g. fig. 2A) shows a bottom heat spreader 110 bonded to the bottom side of the die 102. According to Kahn this type of mounting structure provides an improved thermal, mechanical and electrical performance (col. 1/lls. 52-67; col. 2/lls. 1-6 and col. 3/lls. 14-21).

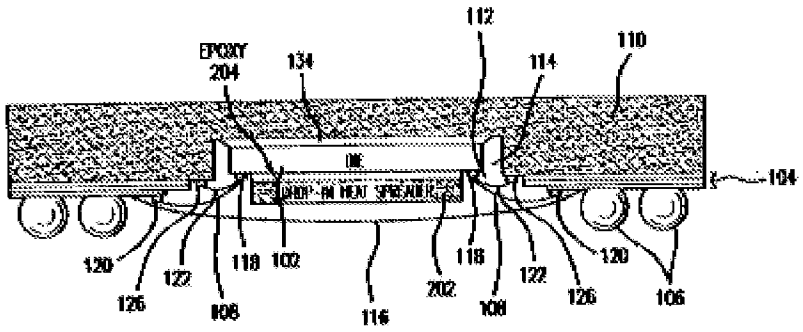


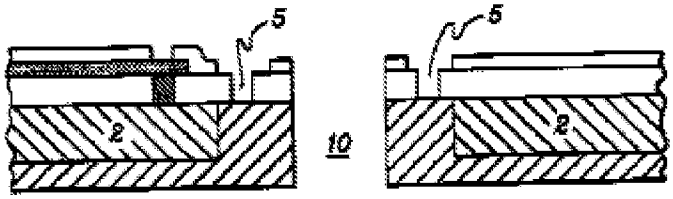
FIG. 2A

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the heat spreader layer of Khan while maintaining the metallurgically bond of Hideshima to improve the thermal, mechanical and electrical performance of the package because more heat can be removed from the circuit due to the shape and size of the heat spreader while maintaining a metallurgically bond because this bond have a low thermal stress due to the fact that the coefficient of thermal expansion of the layers are similar (i.e. Ni, Cu).

Claims 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over anticipated by Hideshima et al. (US 5,143,865) in view of White (US 5,665,655) further in view of Kunikiyo (US 6,717,267).

Regarding claim 15, Hideshima (e.g. fig. 8) shows most aspects of the instant invention including a method of making an integrated circuit system including the steps of:

forming a integrated circuit dice 11 having a top supporting wherein the top supporting exposes electrical signal communication metallization 15/b/e; forming on a bottom side of the dice having a bottom side thermal dissipation metallization 16/45C; but does not include the step of forming multiple die regions on a substrate, forming a top side thermal dissipation metallization and the step of singulating the die regions to form the integrated circuit dices. Nevertheless, White (e.g. figs. 5-8) shows a method including the step of forming multiple die regions on a substrate and the step of singulating the die regions to form the integrated circuit dices. This method increases the yield of devices per wafer because microcrack propagation is reduced (col. 1/lls. 50-55; col. 2/lls. 10-12 & 45-51).



Kunikiyo (e.g. fig. 19) shows the step of forming a topside thermal dissipation metallization 31. According to Kunikiyo, this type of mounting structure provides more satisfactory effect of cooling away the heat in the interlayer insulating films than conventional semiconductor devices having no dummy interconnections or dummy plugs, since metal has higher thermal conducting rate than the interlayer insulating films. This improves the circuit operation of the semiconductor device (col. 23/lls. 1-18). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hideshima's method in accordance to White's teachings which include the step forming multiple die regions on a substrate and the step of the step of singulating the die regions to form the integrated circuit dices to increase the yield of devices per wafer since

microcrack propagations can be reduced and to include the step of forming a topside thermal dissipation metallization such as dummy patterns in the method disclosed by Hideshima in view of White to improve the circuit operation because the heat can be satisfactorily removed form the interlayer insulating films as taught by Kunikiyo.

Regarding claim 16, Hideshima in view of White further in view of teaches that in each die region, the electrical signal communication metallization surrounds the topside thermal dissipation metallization.

Regarding claim 17, Kunikiyo teaches that each topside thermal dissipation metallization comprises an exposed metal layer with an array of through-holes (e.g. 26a).

Regarding claim 18, Kunikiyo (e.g. fig. 19) shows the step of metallurgically bonding a top heat spreader of the package 32 (e.g. 31) to the topside thermal dissipation metallization of the singulated die (dummy pattern 25a).

Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over anticipated by Hideshima et al. (US 5,143,865) in view of White (US 5,665,655) further in view of Kunikiyo (US 6,717,267) further in view of Wang (US 5,977,626).

Regarding claim 19, Hideshima in view of White further in view of Kunikiyo shows most aspects of the instant invention but does not show that the package including a substrate a mounting step comprising the step of mounting the package substrate to the bottom side thermal dissipation metallization of the singulated die. Nevertheless, Wang (e.g. fig. 4) shows a method including a substrate 20 and the step of mounting the bottom side a singulated die 22 to the substrate. This package provides a good efficiency of spreading heat and enhanced EM shielding (col. 1/lls. 11-33; col. 2/lls. 10-14 & col. 3/lls.

10-12). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the method disclosed by Wang to package the device disclosed by Hideshima in view of White further in view Kunikiyo, which includes the step of mounting the bottom side a singulated die to the substrate, because this method produce a package structure having a good efficiency of spreading heat and an enhanced EM shielding as taught by Wang.

(10) Response to Argument

Response to Appellant's arguments A. "Rejection of Claims 1-9 and 21 Under 35 U.S.C. § 103(a) as Unpatentable Over Hideshima et al. (U.S. 5,143,865) in View of Wu (U.S. 2003/0067057)."

Appellant argues that Wu does not constitute a top side thermal dissipation metallization that is supported on the top side of the semiconductor chip 23 because the element 21 does not meet the as definition for "metallization" as present in the specification (see page 4, lines 3-4). The Examiner respectfully disagrees because the element 21 of Wu fully meets Appellant definition of metallization since it is a single- layer metal film formed on an integrated circuit. As shown by figure 3A the layer 21 is an integral component used for heat removal (see pp 009) thus it can be recognized as a "thermal dissipation metallization". Moreover, Appellant argues that the layer 21 of Wu does not support the die. However, the layer 21 is die pad, which is the main function of a die pad. In response to Appellant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight

reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the Appellant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). In this case, Wu teaches that this type of embodiment allows the heat generated from a semiconductor chip to be quickly dissipated through a die pad of the lead frame after the semiconductor chip is attached to the die pad, so as to improve overall heat dissipating efficiency of the semiconductor package (pp 0009).

With regards to Appellant's argument that neither Hideshima et al. nor Wu teaches or suggests anything about supporting thermal dissipation metallizations on both top and bottom sides of a die, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

With regards to Appellant's argument that one skilled in the art at the time the invention was made would not have had a reasonable expectation that the Examiner's proposed modification of Hideshima et al.'s teachings would be successful, it is respectfully note that Wu clearly teaches that that the heat dissipating efficiency of the semiconductor package can be improved by providing a metal layer on the active side (pp 0009). As it is known in the art that some functionalities of the chip are affected by temperature such as speed, circuit operation, operational life, etc, thus it is recommendable to maintain the chip's temperature low by effectively removing the heat

generated at the active area. Therefore, one having ordinarily skills in the art would be motivated to apply Wu's teachings to improve the heat dissipation of the chip disclosed by Hideshima by placing a metallization on the active area.

In response to Appellant's argument that the semiconductor chips disclosed in Hideshima et al. and Wu have different electrical connection needs. As a result, one skilled in the art would have to modify of the teachings of both references in ways that neither reference teaches or suggests in order to arrive at the inventive integrated circuit system as it is defined in claim 1, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). Furthermore, no electrical short-circuit is expected in the combination because die pad is electrically isolated from the active area and from the leads.

With regards to Appellant's argument in connection to claims 8 and 9, that the die pad 21 does not have a through-hole, it is respectfully noted that the metallization layer 21 may have a shape that includes a through hole (see figure 2C).

Response to Appellant's arguments B. "Rejection of Claims 1-4 and 6-11 Under 35 U.S.C. § 103(a) as Unpatentable Over Hideshima et al. (U.S. 5,143,865) in View of Kunikiyo (U.S. 6,717,267)."

Appellant argues that the dummy plugs 31 do not constitute a "metallization" as defined in the specification (page 4, lines 3-4). However, Kunikiyo teaches a metallization layer 30/31 meets Appellant definition of "metallization" because the layer 30/31 is a multi-layer metal film (i.e. horizontally) formed in or on an integrated circuit." Moreover, Appellant argues that the metallizations 31 do not constitute a "thermal dissipation" metallizations in accordance with the ordinary and accustomed meaning of the term "thermal dissipation." In accordance with its ordinary and accustomed meaning, the word "dissipation" refers to the action or process of breaking up and driving off or causing to spread thin or scatter and gradually vanish. (See, e.g., Merriam-Webster's Collegiate Dictionary, 10th ed.). A commonly understood definition of "thermal" is "of, relating to, or caused by heat." (See, e.g., Merriam-Webster's Collegiate Dictionary, 10th ed.). However, it is clear from Kunikiyo's teachings that the metallizations 31 drive off heat by transferring the heat from the circuit to the heat sink 32. Therefore, one having ordinary skills in the art would recognize that the metallization layer is thermal dissipation metallization. In response to Appellant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, this type of mounting structure provides more satisfactory effect of cooling away the heat in the interlayer

insulating films than conventional semiconductor devices having no dummy interconnections or dummy plugs, since metal has higher thermal conducting rate than the interlayer insulating films. This improves the circuit operation of the semiconductor device (see Kunikiyo col. 23/lls. 1-18).

With regards to Appellant's argument that neither Hideshima nor Kunikiyo teaches or suggests anything about supporting thermal dissipation metallizations on both top and bottom sides of a die, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In response to Appellant's argument that neither Hideshima et al. nor Kunikiyo teaches or suggest anything that would have led one skilled in the art at the time the invention was made to incorporate a structure along the lines of Kunikiyo's dummy plugs 31 in the insulating film 17 of Hideshima et al.'s semiconductor device 10, as proposed by the Examiner because Hideshima et al. does not teach or suggest anything about the desirability of a heat-conducting connecting structure along the lines of dummy plugs and dummy interconnections, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

With regards to Appellant's argument that one skilled in the art at the time the invention was made would not have had a reasonable expectation that the Examiner's proposed modification of Hideshima's teachings would be successful, it is respectfully noted that Kunikiyo clearly teaches that the dummy plugs are utilized to promote conduction of heat generated in the interlayer insulating films to the top surface of the semiconductor device so as to enhance the efficiency of cooling the interlayer insulating films (see Kunikiyo col. 22/lls. 28-49). As it is known in the art that some functionalities of the chip are affected by temperature such as circuit operation, speed, operational life, etc thus is recommendable to maintain the chip's temperature low by effectively removing the heat generated at the active area. Therefore, one having ordinarily skills in the art would be motivated to apply Kunikiyo's teachings to improve the heat dissipation of the chip disclosed by Hideshima by placing a metallization on the active area.

With regards to Appellant's argument in connection to claims 8 and 9, that the metallization layer does not have a through-hole, it is respectfully noted that the metallization layer 30/31 includes through holes where the plugs 31 are located.

With reads to Appellant's argument that Kunikiyo does not teach or suggest any specific means by which the heat sink 32 is attached to the plugs 31. The examiner disagrees because Kunikiyo clearly shows a top heat spreader 32 is metallurgically bonded because a metal to metal contact exists (clm. 5). Furthermore, one having ordinary skills in the art would understand that this limitation is implicitly taught because a metal to metal bond is the only alternative to integrally form the structure so as to establish a thermal path between the elements.

Response to Appellant's arguments C: "Rejection of Claims 12 and 13 Under 35 U.S.C. § 103(a) as Unpatentable Over Hideshima et al. (U.S. 5,143,865) in View of Kunikiyo (U.S. 6,717,267), and Further in View of Wang (US. 5,977,626)."

Appellant argues that Kunikiyo does not disclose anything about the means by which the heat sink 32 is attached to the plugs 31. However, Kunikiyo teaches that the heat sink 32 is connected to the plug 31. The limitation "metallurgically bonded" is anticipated because a metal to metal bond exists in the structure. Furthermore, one having ordinary skills in the art would understand that this limitation is implicitly taught because a metal to metal bond is the only alternative to integrally form the structure so as to establish a thermal path between the elements.

Response to Appellant's arguments D.: "Rejection of Claim 14 Under 35 U.S.C. § 103(a) as Unpatentable Over Hideshima et al. (U.S. 5,143,865) in View of Kunikiyo (U.S. 6,717,267), and Further in View of Khan (US. 6,853,070)."

Appellant argues that the prior art does not teach that package further comprises a bottom heat spreader metallurgically bonded to the bottom side thermal dissipation metallization of the die because Khan teaches that the heat spreader 110 is attached to the bottom side of the die 102 using an epoxy. (See Khan, col. 4, lines 60-61). Nevertheless, Hideshima shows that the package further comprises a bottom layer 45C metallurgically bonded (i.e. metal to metal bond) to the bottom side thermal dissipation metallization 16. Hideshima does not explicitly disclose that the second layer 45C is a heat spreader. In that regards, Khan (e.g. fig. 2A) shows a bottom heat spreader 110. It is respectfully noted that one of ordinary skills in the art would keep the metal to metal bond

disclosed by Hideshima because this type of bond has a low thermal stress since the coefficient of thermal expansion of the nickel layer 16 is relatively similar to the one of copper (heat sink).

Response to Appellant's arguments E. "Rejection of Claims 15-18 Under 35 U.S.C. § 103(a) as Unpatentable Over Hideshima et al. (U.S. 5,143,865) in View of White (U.S. 5,665,655), and Further in View of Kunikiyo (U.S. 6,717,267)."

With respect to claim 15, Appellant's argues that neither Hideshima. nor Kunikiyo teaches or suggests at least "forming on a top side of a substrate . . . an exposed top side thermal dissipation metallization .... " Therefore, claim 15 is patentable over Hideshima et al., White and Kunikiyo for at least the same reasons explained above in connection with independent claim 1. Nevertheless, Kunikiyo (e.g. fig. 19) shows the step of forming a topside thermal dissipation metallization 31.

With respect to Appellant argument that there is no support for the Examiner's assertion that the heat sink 32 is metallurgically bonded to the plug 31. It is respectfully noted that the limitation "metallurgically bonded" is anticipated because a metal to metal bond exists in the structure disclosed by Kunikiyo. Furthermore, one having ordinary skills in the art would understand that this limitation is implicitly disclosed because a metal to metal bond is the only alternative to integrally form the structure so as to establish a thermal path between the elements.

Regarding Appellant's arguments F: "Rejection of Claims 19 and 20 Under 35 U.S.C. § 103(a) as Unpatentable Over Hideshima et al. (U.S. 5,143,865) in View of White

(U.S. 5,665,655) and Kunikiyo (U.S. 6,717,267), and Further in View of Wang (U.S. 5,977,626)."

With respect to Appellant's argument that Kunikiyo does not teach or suggest anything about attaching the heat sink 32 to the plug 31. Therefore, there is no support for the Examiner's assertion that the heat sink 32 is metallurgically bonded to the plug 31. It is respectfully noted that the limitation "metallurgically bonded" is anticipated because a metal to metal bond exists in the structure disclosed by Kunikiyo (see clm 5). Furthermore, one having ordinary skills in the art would understand that this limitation is implicitly disclosed because a metal to metal bond is the only alternative to integrally form the structure so as to establish a thermal path between the elements.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Leonardo Andújar/
Primary Examiner, Art Unit 2826

Conferees:
/Sue A Purvis/
Supervisory Patent Examiner, Art Unit 2826

/Ricky L. Mack/
Supervisory Patent Examiner, Art Unit 2873